IDEC Chip Design Contest

A 40-Gb/s NRZ Mixed-Signal Receiver With 2-Tap FFE and 1-Tap DFE

Kee-Bong Hyun, Tae-Young Choi, Dong-Hyeon Kim and Woo-Young Choi

Introduction

- ❖ High-speed electrical links for AI/HPC and cloud data-center systems require reliable binary data transfer over lossy PCB and cable channels.
- ❖ At 40 Gb/s, NRZ signaling suffers from severe ISI over high-loss channels, requiring a careful equalization partition beyond simple front-end peaking.
- ❖ This work presents a 40-Gb/s NRZ mixed-signal receiver in 28-nm CMOS using a level-shifter-assisted two-stage T/H, a 2-tap RX FFE, and a 1-tap direct DFE for equalization over a 32-dB-loss channel.

Behavioral Modeling

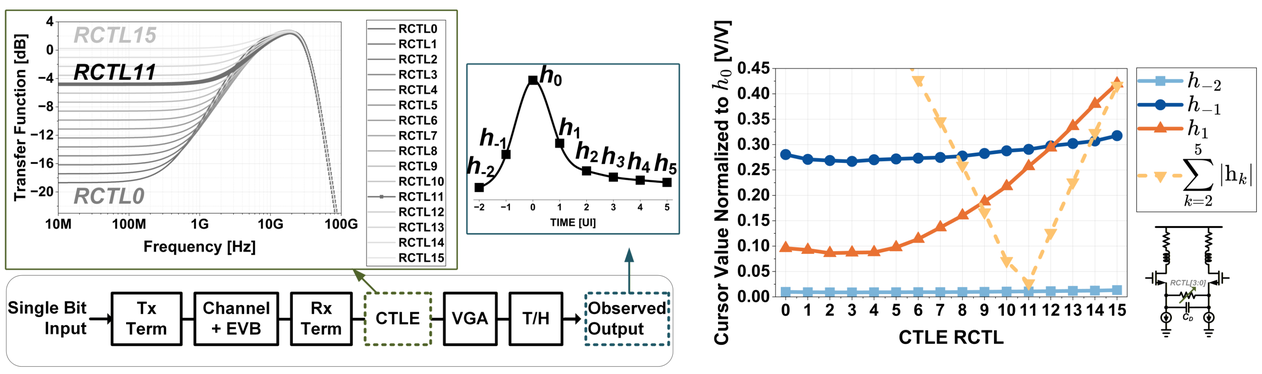


Fig. 1. Behavioral modeling used to determine equalization partition.

- ❖ The CTLE suppresses long-tail post-cursor ISI, while the 1-tap direct DFE cancels the residual 1st post-cursor.
- ❖ The 2-tap RX FFE compensates for the dominant 1st pre-cursor without imposing the timing burden of a 3-tap RX FFE.

Circuit Implementation

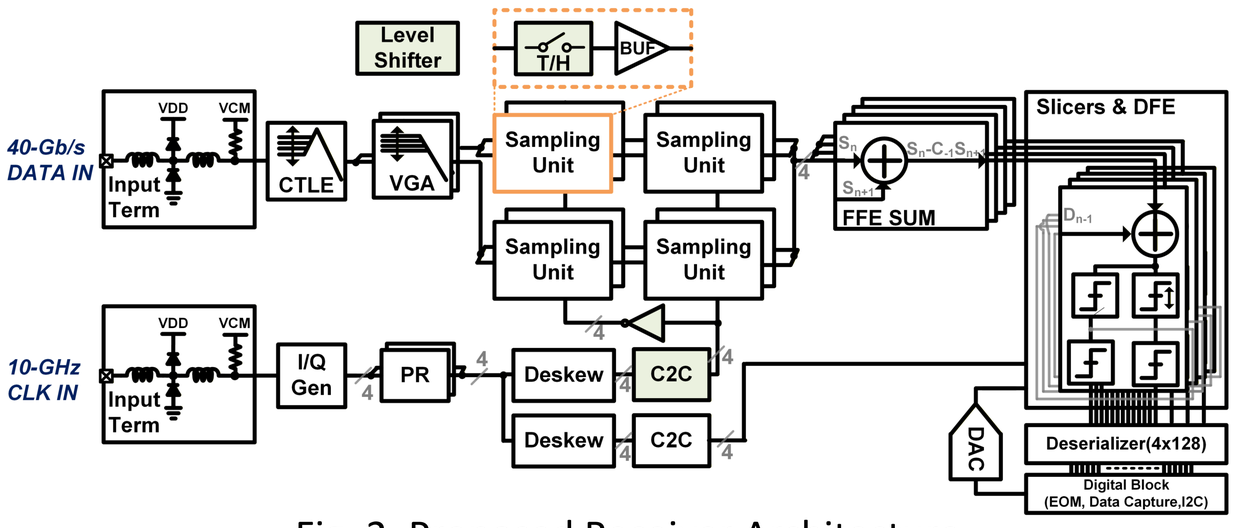
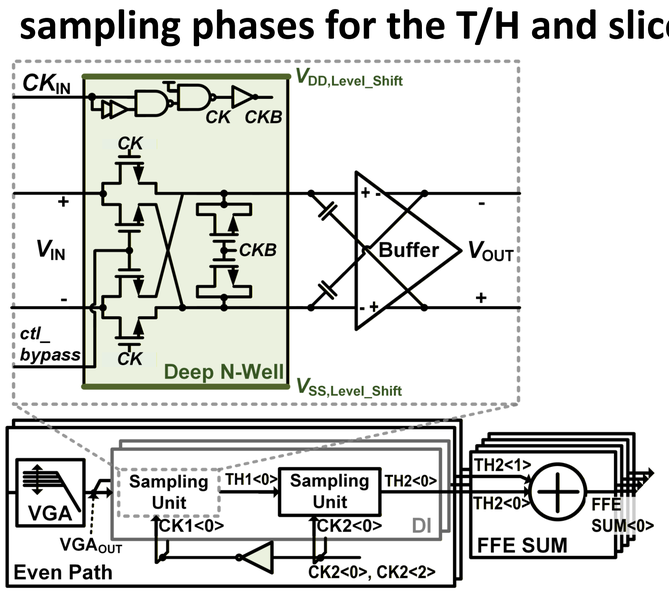


Fig. 2. Proposed Receiver Architecture

- ❖ The proposed receiver adopts a 4-way time-interleaved quarter-rate architecture, where a 10-GHz external clock generates four sampling phases for the T/H and slicer paths.



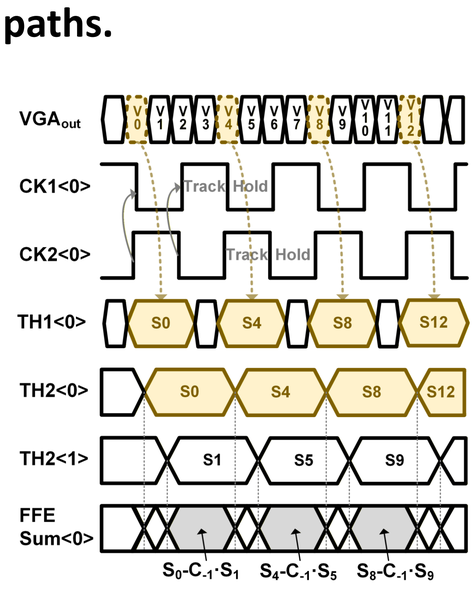


Fig. 3. Two-stage T/H path and timing diagram for the 2-tap RX FFE.

- ❖ The level-shifter-assisted T/H reduces input-dependent sampling errors, while reduced-aperture timing suppresses charge-sharing-induced ISI before 2-tap RX FFE summation.

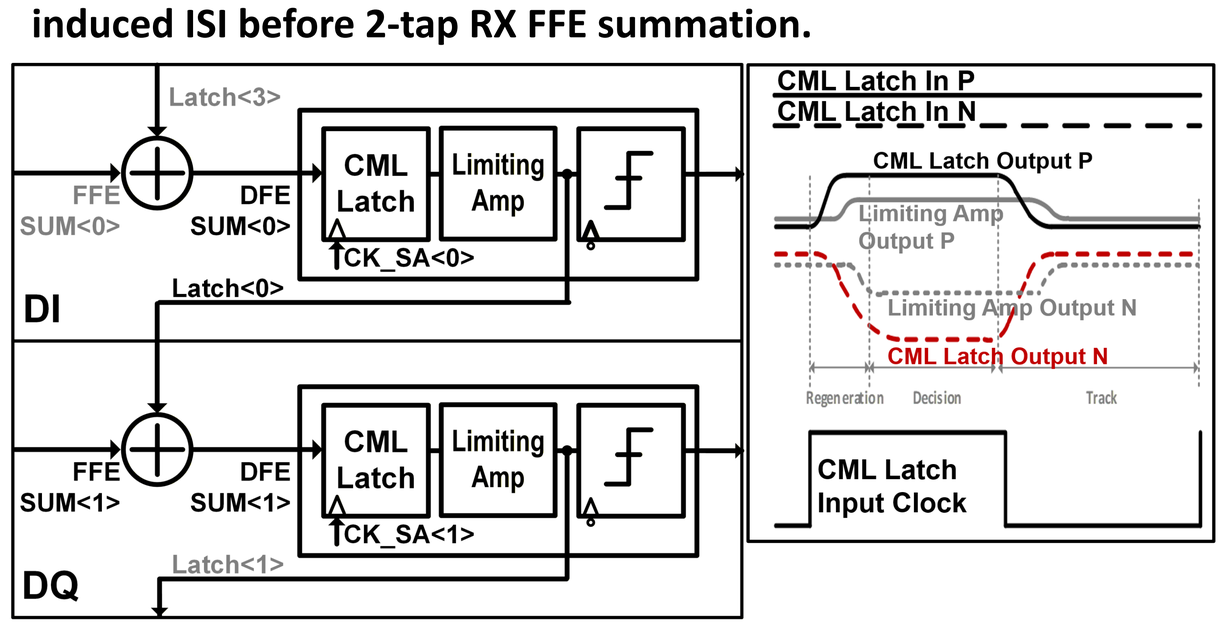


Fig. 4. DFE loop and slicer timing

- ❖ The DFE latch pre-amplifies the held FFE-summed input and partially establishes the DFE feedback current before regeneration, enabling fast first-tap direct DFE settling.

Measurement Results

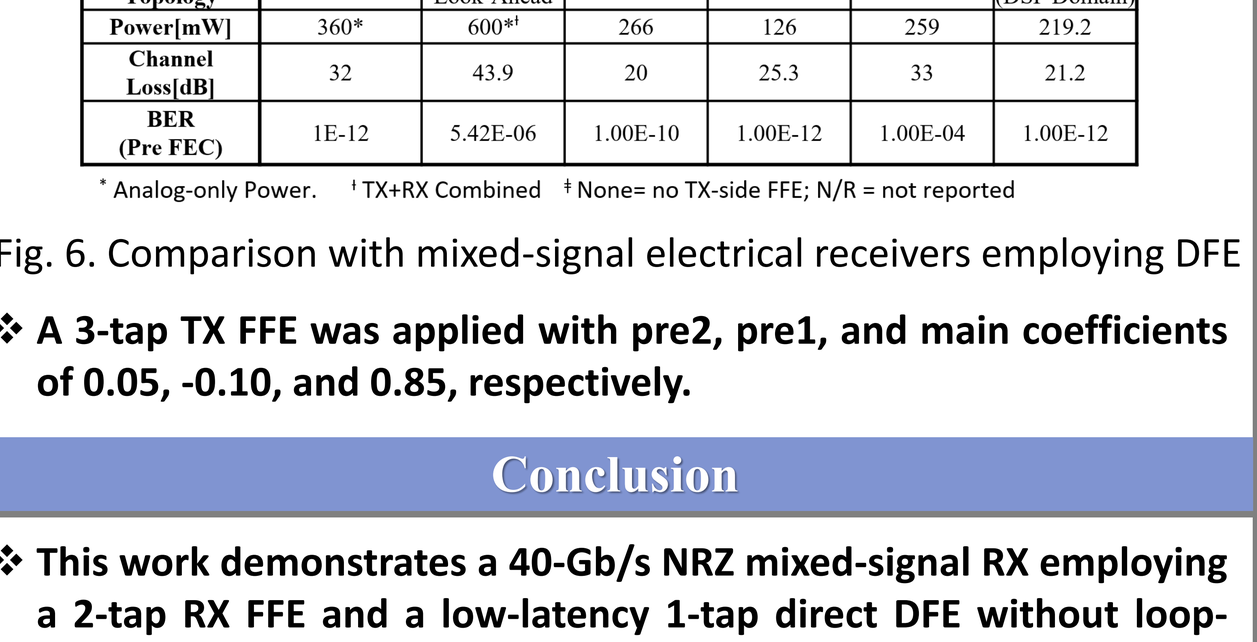


Fig. 5. Measured channel loss and 40-Gb/s NRZ bathtub curves

Index	This Work	JSSC 2024	TCAS-I 2021	TCAS-I 2024	ISSCC 2022	ISSCC 2025
Technology	28nm	7nm	65nm	28nm	10nm	28nm
Data Rate [Gbps]	40	112	56	50	58.125	106.25
Modulation	NRZ	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4
Rx Equalization	CTLE 1-Tap DFE 2-Tap FFE	2-Stage CTLE 3-Tap FFE 18-Tap DFE	CTLE 4-tap DFE	2-Stage CTLE 2-tap DFE	3-stage CTLE 16-tap DFE	CTLE 1-tap DFE 3-tap FFE
Tx FFE in Evaluated Link‡	3-Tap	6-Tap	2-Tap	None	N/R	None
DFE Topology	Direct	1+D Shape Look-Ahead	Direct	Direct	Direct	Speculative (DSP Domain)
Power[mW]	360*	600*†	266	126	259	219.2
Channel Loss[dB]	32	43.9	20	25.3	33	21.2
BER (Pre FEC)	1E-12	5.42E-06	1.00E-10	1.00E-12	1.00E-04	1.00E-12

* Analog-only Power. † TX+RX Combined ‡ None= no TX-side FFE; N/R = not reported

Fig. 6. Comparison with mixed-signal electrical receivers employing DFE

- ❖ A 3-tap TX FFE was applied with pre2, pre1, and main coefficients of 0.05, -0.10, and 0.85, respectively.

Conclusion

- ❖ This work demonstrates a 40-Gb/s NRZ mixed-signal RX employing a 2-tap RX FFE and a low-latency 1-tap direct DFE without loop-unrolled DFE overhead in 28-nm CMOS.
- ❖ The prototype achieves <1E-12 BER at 40 Gb/s over a 32-dB-loss channel with 3-tap TX FFE in the evaluated link.